**Moore Machine State Diagram for ATM:**

Basically FSM is a representation of the different transition taken place in a system. A state machine is an effective way to implement the control functions. The Moore Machine for the overall ATM controller is represented in fig.4.2. The description of state code and state input signal are tabulated in table 4.1 and table 4.2.

***Operation:***

Initially the system is in idle state and when it is ready to operate, S0 state is selected which represents the scan card. When the user gets the card inserted, scan line goes high which represents the next state S1. If the card line goes low, control signal will return back to the scan card state. In state S2, card number and pin number is stored in the registers. If any error occurs in storing the card information, the signal will go the state S0.

After storing the card information, control signal will leads to the screen in which the user allowed to enter the pin which is represented by the state S3. When the invalid pin is entered, signal will again goes to state S3 and allow the user to enter pin again. The counter will be installed which is represented as S4 state, to count the number of trials. If it exceeds three times, the account gets locked and control signal return to scan card (S0) state.

When the valid pin is entered i.e. pin get matched, control signal will lead to the state S5 in which user can select the transaction type.

There are two types of transaction can be made as follows.

1. Deposit
2. Withdraw

Deposit state is represented by S6 in which the user allowed to deposit the amount through amount entering. User will be taken again to transaction type screen by making cancel deposit to high.

The amount entered will be added with the old balance that stored in memory and checked whether it overflow 16bit, represented by state S7. If balance get overflowed, control signal will go to invalid state S8 and then to anything else state S9. The state S10 represents entered amount is valid and is verified. Once verification is over, the updating of balance is made which is represented by the state S11. After updating, the signal will goes to the anything else state S9 from which user will be allowed to make more transaction by taking to state S5 else to the state S0.

Fig.4.2 Moore Machine Diagram for ATM Controller

IC=1

1

CS=1

AU=1

AU=0

CS=0

IPin=1

IPin=0

PM=1

OP=0

OP=1

AE=0

AE=0

AE=1

VT=1

AE=1

VT=1

TV=1

TV=0

VT=0

MT=1

MT=0

VT=0

TV=1

TV=0

PM=0

Reset

IC=0

Withdraw state is represented by S12 in which the user allowed to enter the withdraw amount from his account. If the withdraw process is cancelled, signal will again goes to the transaction type state S5 else the amount entered will be checked through the state S13.

**Table 4.1 State Code Descriptions**

|  |  |
| --- | --- |
| State Code | State Description |
| S0 | Scan Card |
| S1 | Scan Line |
| S2 | Storing information |
| S3 | Enter PIN |
| S4 | Count |
| S5 | Transaction type |
| S6 | Enter Deposit Amount |
| S7 | Deposit Check |
| S8 | Invalid |
| S9 | Anything Else |
| S10 | Deposit Verify |
| S11 | Updating Balance |
| S12 | Enter Withdraw Amount |
| S13 | Withdraw Check |
| S14 | Withdraw Verify |

**Table 4.2 Table showing input signals**

|  |  |
| --- | --- |
| Signal Code | Signal Description |
| IC | Insert Card |
| CS | Card Scan |
| AU | Account Unlocked |
| PM | PIN Matched |
| IPin | Invalid Pin Count |
| OP | Option Select |
| AE | Amount Entered |
| VT | Valid Transaction |
| MT | More Transaction |
| TV | Transaction Verified |

After checking process will be carried out, if amount entered is invalid, control signal will go to invalid state S8 and from which signal goes to another transaction state S9. If the entered amount is valid, then state S14 will be processed which will verify the amount and leads to the updating balance state S11. In this state, the amount will get updated in memory. After updating, user is taken to another transaction state S9 from which he can make more transaction else taken to scan card state.